

We claim:

1. A method for forming ultra shallow junctions, comprising:

5       providing a semiconductor;

          implanting a dopant species into said semiconductor; and

          annealing said implanted semiconductor with a ultra high  
10   temperature anneal comprising annealing temperatures from 1050°C  
to 1350°C.

2. The method of claim 1 further comprising an amorphizing  
implant.

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3. The method of claim 2 wherein said amorphizing implant  
comprises implanting a species from the group consisting of  
silicon, germanium, antimony, indium, arsenic, neon, argon,  
krypton, and xenon.

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4. The method of claim 1 wherein said ultra high temperature  
anneal comprises times from 0.5 milliseconds to 3 milliseconds.

5. A method for forming junction in integrated circuits,  
comprising:

providing a semiconductor;

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forming a patterned photoresist layer on said  
semiconductor;

implanting dopant species into said semiconductor;

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removing said patterned photoresist layer;

annealing said implanted semiconductor with a solid phase  
epitaxy anneal; and

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annealing said implanted semiconductor with a ultra high  
temperature anneal comprising annealing temperatures from 1100°C  
to 1350°C.

20 6. The method of claim 5 wherein said ultra high temperature  
anneal comprises times from 0.5 milliseconds to 3 milliseconds.

7. The method of claim 6 further comprising an amorphizing implant.

8. The method of claim 7 wherein said amorphizing implant  
5 comprises implanting a species from the group consisting of  
silicon, germanium, antimony, indium, arsenic, neon, argon,  
krypton, and xenon.

9. A method of forming a MOS transistor, comprising:

providing a semiconductor substrate;

5       forming a gate dielectric layer on said semiconductor;

forming a gate electrode on said gate dielectric layer;

10       implanting dopant species into said semiconductor adjacent  
to said gate electrode;

annealing said implanted semiconductor with a solid phase  
epitaxy anneal at a temperature between 550°C and 950°C; and

15       annealing said implanted semiconductor with a ultra high  
temperature anneal comprising annealing temperatures from 1100°C  
to 1350°C.

10. The method of claim 9 wherein said ultra high temperature  
20       anneal comprises times from 0.5 milliseconds to 3 milliseconds.

11. The method of claim 10 further comprising an amorphizing implant performed prior to said implanting of said dopant species.

5 12. The method of claim 11 wherein said amorphizing implant comprises implanting a species from the group consisting of silicon, germanium, antimony, indium, arsenic, neon, argon, krypton, and xenon.

13. A method of forming an integrated circuit MOS transistor,  
comprising:

providing a semiconductor substrate;

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forming a gate dielectric layer on said semiconductor;

forming a gate electrode on said gate dielectric layer;

10       implanting first dopant species into said semiconductor  
adjacent to said gate electrode;

forming sidewall structures adjacent to said gate  
electrode;

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implanting second dopant species into said semiconductor  
adjacent to said sidewall structures; and

annealing said implanted semiconductor with a ultra high  
20   temperature anneal comprising annealing temperatures from 1100°C  
to 1350°C.

14. The method of claim 13 wherein said ultra high temperature  
anneal comprises times from 0.5 milliseconds to 3 milliseconds.

15. The method of claim 14 further comprising an amorphizing  
implant performed prior to said implanting of said first dopant  
5 species.

16. The method of claim 15 further comprising an amorphizing  
implant performed prior to said implanting of said second dopant  
species.

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17. The method of claim 13 further comprising an amorphous  
implant performed prior to said implanting of said second dopant  
species.

15 18. The method of claim 16 wherein said amorphizing implants  
comprises implanting a species from the group consisting of  
silicon, germanium, antimony, indium, arsenic, neon, argon,  
krypton, and xenon.